

What is claimed is:

1 1. A computer implemented method for functionally abstracting a memory
2 column, comprising:

3 identifying, in a description of a circuit, at least one column of n memory cells,
4 where n is an integer greater than 1;

5 representing said column of n memory cells as a single-memory-cell column
6 comprising a single representative memory cell;

7 abstracting at least a portion of said single-memory-cell column to derive a logic-
8 level representation for said representative memory cell; and

9 generating one or more additional instances of said logic-level representation to
10 derive an abstracted memory column comprising a plurality of instances of said logic-
11 level representation.

1 2. The method of claim 1, wherein said logic-level representation comprises
2 a latch.

1 3. The method of claim 2, wherein generating one or more additional
2 instances comprises:

3 generating n-1 additional instances of said logic-level representation to derive an
4 abstracted memory column comprising n instances of said logic-level representation.

1 4. The method of claim 1, wherein abstracting comprises:
2 deriving a gate-level representation for said representative memory cell; and

3 abstracting a latch from at least a portion of said gate-level representation.

1 5. The method of claim 4, wherein deriving a gate-level representation
2 comprises:

3 applying symbolic analysis to a transistor level description of said representative
4 memory cell.

1 6. The method of claim 1, wherein identifying a column of n memory cells
2 comprises:

3 verifying that all of said n memory cells are substantially identical in structure
4 relative to each other.

1 7. The method of claim 6, further comprising:

2 selecting one of said n memory cells to be said representative memory cell.

1 8. The method of claim 7, wherein representing said column of n memory
2 cells as a single-memory-cell column comprises:

3 removing all of said n memory cells except for said representative memory cell
4 from said column.

1 9. The method of claim 1, wherein said representative memory cell is
2 initially coupled to a particular select line, and wherein representing said column of n
3 memory cells as a single-memory-cell column comprises:

4 decoupling said representative memory cell from said particular select line.

1 10. The method of claim 9, wherein abstracting said single-memory-cell
2 column comprises:

3 coupling said logic-level representation of said representative memory cell to said
4 particular select line.

1 11. The method of claim 1, wherein generating additional instances of said
2 logic-level representation comprises:

3 generating one or more additional instances of said logic-level representation; and
4 for each additional instance generated, coupling that instance to a distinct select
5 line.

1 12. The method of claim 11, wherein generating additional instances of said
2 logic-level representation further comprises:

3 making an explicit assumption that selection of each select line is mutually
4 exclusive relative to all other select lines.

1 13. The method of claim 1, wherein said abstracted memory column is cycle
2 ready.

1 14. An apparatus for functionally abstracting a memory column, comprising:

2 a mechanism for identifying, in a description of a circuit, at least one column of n
3 memory cells, where n is an integer greater than 1;
4 a mechanism for representing said column of n memory cells as a single-memory-
5 cell column comprising a single representative memory cell;
6 a mechanism for abstracting at least a portion of said single-memory-cell column
7 to derive a logic-level representation for said representative memory cell; and
8 a mechanism for generating one or more additional instances of said logic-level
9 representation to derive an abstracted memory column comprising a plurality of instances
10 of said logic-level representation.

1 15. The apparatus of claim 14, wherein said logic-level representation
2 comprises a latch.

1 16. The apparatus of claim 15, wherein the mechanism for generating one or
2 more additional instances comprises:
3 a mechanism for generating n-1 additional instances of said logic-level
4 representation to derive an abstracted memory column comprising n instances of said
5 logic-level representation.

1 17. The apparatus of claim 14, wherein the mechanism for abstracting
2 comprises:
3 a mechanism for deriving a gate-level representation for said representative
4 memory cell; and

5 a mechanism for abstracting a latch from at least a portion of said gate-level
6 representation.

1 18. The apparatus of claim 17, wherein the mechanism for deriving a gate-
2 level representation comprises:

3 a mechanism for applying symbolic analysis to a transistor level description of
4 said representative memory cell.

1 19. The apparatus of claim 14, wherein the mechanism for identifying a
2 column of n memory cells comprises:

3 a mechanism for verifying that all of said n memory cells are substantially
4 identical in structure relative to each other.

1 20. The apparatus of claim 19, further comprising:

2 a mechanism for selecting one of said n memory cells to be said representative
3 memory cell.

1 21. The apparatus of claim 20, wherein the mechanism for representing said
2 column of n memory cells as a single-memory-cell column comprises:

3 a mechanism for removing all of said n memory cells except for said
4 representative memory cell from said column.

1 22. The apparatus of claim 14, wherein said representative memory cell is
2 initially coupled to a particular select line, and wherein the mechanism for representing
3 said column of n memory cells as a single-memory-cell column comprises:
4 a mechanism for decoupling said representative memory cell from said particular
5 select line.

1 23. The apparatus of claim 22, wherein the mechanism for abstracting said
2 single-memory-cell column comprises:
3 a mechanism for coupling said logic-level representation of said representative
4 memory cell to said particular select line.

1 24. The apparatus of claim 14, wherein the mechanism for generating
2 additional instances of said logic-level representation comprises:
3 a mechanism for generating one or more additional instances of said logic-level
4 representation; and
5 a mechanism for coupling, for each additional instance generated, that instance to
6 a distinct select line.

1 25. The apparatus of claim 24, wherein the mechanism for generating
2 additional instances of said logic-level representation further comprises:
3 a mechanism for making an explicit assumption that selection of each select line
4 is mutually exclusive relative to all other select lines.

1 26. The apparatus of claim 14, wherein said abstracted memory column is
2 cycle ready.

1 27. A computer readable medium, comprising:
2 instructions for causing one or more processors to identify, in a description of a
3 circuit, at least one column of n memory cells, where n is an integer greater than 1;
4 instructions for causing one or more processors to represent said column of n
5 memory cells as a single-memory-cell column comprising a single representative
6 memory cell;
7 instructions for causing one or more processors to abstract at least a portion of
8 said single-memory-cell column to derive a logic-level representation for said
9 representative memory cell; and
10 instructions for causing one or more processors to generate one or more additional
11 instances of said logic-level representation to derive an abstracted memory column
12 comprising a plurality of instances of said logic-level representation.

1 28. The computer readable medium of claim 27, wherein said logic-level
2 representation comprises a latch.

1 29. The computer readable medium of claim 28, wherein the instructions for
2 causing one or more processors to generate one or more additional instances comprises:

3 instructions for causing one or more processors to generate n-1 additional
4 instances of said logic-level representation to derive an abstracted memory column
5 comprising n instances of said logic-level representation.

1 30. The computer readable medium of claim 27, wherein the instructions for
2 causing one or more processors to abstract comprises:

3 instructions for causing one or more processors to derive a gate-level
4 representation for said representative memory cell; and
5 instructions for causing one or more processors to abstract a latch from at least a
6 portion of said gate-level representation.

1 31. The computer readable medium of claim 30, wherein the instructions for
2 causing one or more processors to derive a gate-level representation comprises:
3 instructions for causing one or more processors to apply symbolic analysis to a
4 transistor level description of said representative memory cell.

1 32. The computer readable medium of claim 27, wherein the instructions for
2 causing one or more processors to identify a column of n memory cells comprises:
3 instructions for causing one or more processors to verify that all of said n memory
4 cells are substantially identical in structure relative to each other.

1 33. The computer readable medium of claim 32, further comprising:

2 instructions for causing one or more processors to select one of said n memory
3 cells to be said representative memory cell.

1 34. The computer readable medium of claim 33, wherein the instructions for
2 causing one or more processors to represent said column of n memory cells as a single-
3 memory-cell column comprises:

4 instructions for causing one or more processors to remove all of said n memory
5 cells except for said representative memory cell from said column.

1 35. The computer readable medium of claim 27, wherein said representative
2 memory cell is initially coupled to a particular select line, and wherein the instructions
3 for causing one or more processors to represent said column of n memory cells as a
4 single-memory-cell column comprises:

5 instructions for causing one or more processors to decouple said representative
6 memory cell from said particular select line.

1 36. The computer readable medium of claim 35, wherein the instructions for
2 causing one or more processors to abstract said single-memory-cell column comprises:
3 instructions for causing one or more processors to couple said logic-level
4 representation of said representative memory cell to said particular select line.

1 37. The computer readable medium of claim 27, wherein the instructions for
2 causing one or more processors to generate additional instances of said logic-level
3 representation comprises:

4 instructions for causing one or more processors to generate one or more additional
5 instances of said logic-level representation; and
6 instructions for causing one or more processors to couple, for each additional
7 instance generated, that instance to a distinct select line.

1 38. The computer readable medium of claim 37, wherein the instructions for
2 causing one or more processors to generate additional instances of said logic-level
3 representation further comprises:

4 instructions for causing one or more processors to make an explicit assumption
5 that selection of each select line is mutually exclusive relative to all other select lines.

1 39. The computer readable medium of claim 27, wherein said abstracted
2 memory column is cycle ready.